What is claimed is:

1. A liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the liquid crystal display device comprising:

means disposed at intervals of M (positive integer) lines of the data signal lines for selecting N (positive integer, M >= N) data signal lines from the M data signal lines and comparing voltages of the N data signal lines.

2. The liquid crystal display device as set forth in claim 1, further comprising:

detecting means connected to the comparing means for detecting defective pixels.

3. The liquid crystal display device as set

forth in claim 2,

wherein the detecting means is composed of exclusive OR means.

4. The liquid crystal display device as set forth in claim 1, further comprising:

data converting means connected to the comparing means for converting parallelly supplied data into serial data and outputting the serial data.

5. The liquid crystal display device as set forth in claim 1,

wherein M and N are 2 each.

6. A liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the liquid crystal display device comprising:

means disposed at intervals of two of the data signal lines for comparing voltages of the two data signal lines.

7. The liquid crystal display device as set forth in claim 6, further comprising:

exclusive OR means connected to the comparing means.

8. The liquid crystal display device as set forth in claim 6, further comprising:

data converting means connected to the comparing means for converting parallelly supplied data into serial data and outputting the serial data.

9. A liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the liquid crystal display device

comprising:

a plurality of auxiliary data signal lines disposed corresponding to the data signal lines and connected to the output electrodes of the respective pixel transistors; and

calculating means connected to one of the auxiliary data signal lines and one of the gate signal lines.

10. A method for inspecting a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the method comprising the steps of:

supplying two predetermined different voltages to two adjacent data signal lines and storing the two predetermined different voltages to capacitors connected to the two signal lines through the

respective pixel transistors; and

comparing voltages that are read from the capacitors to the two data signal lines.

11. A method for inspecting a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the method comprising the steps of:

supplying different voltages to two data signal lines and storing the two different voltages to the capacitors through the respective pixel transistors connected to the two data signal lines;

pre-charging a reference potential to all the data signal lines and reading voltages stored in the capacitors to the two data signal lines; and

comparing the voltages of the two data signal lines.

12. The method as set forth in claim 11, further comprising the step of:

inverting the voltages applied to the two data signal lines and performing the supplying step, the pre-charging step, and the comparing step in succession.